CLAIMS:

1. Method for manufacturing on a substrate a semiconductor device with a floating-gate and a control-gate, comprising the steps of:

- first forming isolation zones in the substrate,
- thereafter forming a floating gate on the substrate between two isolation zones,
- thereafter extending the floating gate using conductive spacers, and
- thereafter forming a control gate over the floating gate and the conductive spacers.

2. Method according to claim 1, wherein the step of forming the floating gate comprises:

- providing the floating gate on the substrate, the floating gate having two opposite walls located above the isolation zones,
- forming a recess in the isolation zones under the opposite walls of the floating gate.

3. Method according to claim 2, wherein the step of providing the floating gate, comprises:

- depositing a floating gate layer
- forming slits in the floating gate layer, thus forming the opposite walls of the floating gate.

4. Method according to claim 2, wherein the step of extending the floating gate comprises depositing a conductive layer on the opposite walls of the floating gate and on the walls of the recess in the isolation zones.

5. Method according to claim 4, wherein the step of depositing a conductive layer on the opposite walls of the floating gate and on the walls of the recesses in the isolation zones comprises:

- depositing a conductive layer over the floating gate and in the recesses in the isolation zones
- etching the conductive layer.

6. Method according to claim 1, further comprising a step of forming a dielectric layer on the floating gate and on the conductive spacers before forming the control gate.

7. Method according to claim 1, wherein the isolation zones are shallow trench isolation (STI) zones.

8. Method according to claim 1, wherein the isolation zones are LOCOS regions.

9. Method according to claim 2, wherein a recess in an isolation zone is formed by etching.

10. Method according to claim 1, comprising the step of providing a tunnel oxide between the semiconductor substrate and the floating gate.

11. Method according to claim 1, wherein the step of forming the control gate comprises:
- depositing a control gate layer, and
- patterning the control gate layer to form the control gate.

12. Method according to claim 1, wherein the conductive spacers are polysilicon spacers.

13. Semiconductor device with a floating-gate to control-gate coupling ratio, comprising:
- a substrate with a planar surface,
- two isolation zones in the substrate in the planar surface,
- a floating gate on the substrate between two isolation zones, the floating gate having two side walls extending vertically with respect to the planar surface of the substrate, the walls having a height as measured from the planar surface,

- conductive spacers extending the floating gate from each wall laterally with respect to the planar surface, the conductive spacers extending vertically with respect to the planar surface at least over the height of the floating gate side walls, and

- a control gate extending laterally with respect to the planar surface over the floating gate and the conductive spacers.

14. Semiconductor device according to claim 13, wherein the conductive spacers furthermore extend vertically with respect to the planar surface over a supplementary height in a recess below the surface.

15. An array of semiconductor devices of any of claims 13 or 14, wherein there is a sub-lithographic slit between floating gates of adjacent semiconductor devices.

16. A non-volatile memory including the semiconductor device according to any of the claims 13 or 14.

17. The non-volatile memory according to claim 16, wherein the memory is a flash memory.

18. The non-volatile memory according to claim 16, wherein the memory is an EEPROM.